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U.S. Patent Documents

Examiner Initial		DOCUMENT NUMBER	DATE	NAME	CLA SS	SUBC LASS	FILING DATE

Foreign Patent Documents

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							YES	No
PC		2002-313951	4/11/2001	Japan			Abstract	X

Other Documents (Including Author, Title, Date Pertinent Pages, Etc.)

PC	Digh Hisamoto, "FD/DG-SOI MOSFET – A Viable Approach to Overcoming the Device Scaling Limit", IEEE (2001), 4 pages
	Robert Chau et al., "30 nm Physical Gate Length CMOS Transistors with 1.0 ps n-MOS and 1.7 ps p-MOS Gate Delays", IEEE (2000), 4 pages
	Patrick P. Gelsinger, "Microprocessors for the New Millennium: Challenges, Opportunities, and New Frontiers", 2001 IEEE International Solid-State Circuits Conference, 10 pages
	D.A. Buchanan et al. "80 nm Poly-silicon Gated n-FETs with Ultra-Thin Al ₂ O ₃ Gate Dielectric for ULSI Applications", IEEE (2000), 4 pages
	K. Torii et al., "Fixed Charge-Induced Mobility Degradation and its Recovery in MISFET's with Al ₂ O ₃ Gate Dielectric", IWGI 2001, Tokyo, pp. 230-232
	K. Torii et al., "The Mechanism of Mobility Degradation in MISFETs with Al ₂ O ₃ Gate Dielectric", IEEE, 2002 Symposium on VLSI Technology Digest of Technical Papers, 2 pages
	K. Rim et al., "Mobility Enhancement in Strained Si NMOSFETs with HfO ₂ Gate Dielectrics", IEEE, 2002 Symposium on VLSI Technology Digest of Technical Papers, 2 pages
↓	Kunihiro Suzuki et al., "Scaling Theory for Double-Gate SOI MOSFET's", IEEE Transactions on Electron Devices, Vol. 40, No. 12, December 1993, pp. 2326-2329
PC	International Technology Roadmap for Semiconductors, 2001 Edition, "Front End Processes", pp. I-44
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	DATE CONSIDERED 05/12/2006

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